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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,639	09/05/2003	Paul Durrant	SUN-P7783	8119

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EXAMINER	
CAMPOS, YAIMA	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 11/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,639	DURRANT, PAUL	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/656,639 has a total of 27 claims pending in the application; there are 2 independent claims and 25 dependent claims, all of which are ready for examination by the examiner. At this point claims 13, 21 and 28 have been cancelled.

I. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-4, 9-10, 14-20 ,22-25 and 29-30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Garret et al. (US 6,408,369) in view of McKenney (US 6,230,241) and Fujihira et al. (US 5,278,965).

4. As per **claims 1 and 22**, Garret discloses "a computer system including

a processor" **[Garret discloses that "the system further comprises a control processor" (Column 1, lines 48-49) and "Hosts 12a-12n" (Figure 1)]**

"a first controller" **[With respect to this limitation, Garret disclose "Memory controller 14" (Figure 1)]**

a memory having a plurality of locations for storing data **["Disk drives 16a-16k" and "Tape storage devices 18a-18k" (Figure 1)]**

"a data communications facility interconnecting said processor, said first controller, and said random access memory;" **["Busses 36" (Figure 1)]**

wherein said first controller is responsive to a command received from the processor to commence transmission of a quantity of data from a first memory location to a second memory location, wherein said command specifies said first and second memory locations **[With respect to this limitation, Garret discloses a system and method featuring the "transfer of data from a first storage device to a second storage device" (Column 1, lines 34-35) where "the controller receives a transfer command from the outside source" (Column 1, lines 48-50) which is specified to be a processor (Column 1, lines 38-39). It is inherent that a command that's moving data from one memory location to another must have both, the source and destination locations included in the command. (Reference cited for inherency in section VII)].**

Garret does not expressly disclose that the memory system in claim 1 is a random access memory for volatile storage of data and "with the first controller monitoring operation of the processor to terminate the transmission of the data to the second randome access memory location, during transmission of the quantity thereto, in response to the processor generating a write request to the second random memory location."

McKenney discloses performing internal transfer of data within a random access volatile storage as **[a system to internally "transfer data between a source and a destination memory" (Column 1, lines 6-9) which may be either main memory or I/O memory (Column 9, lines 19-33); wherein "the central processing unit instructs the cache memory unit to map source and destination locations in the cache memory unit to respective portions of the source and destination memory units in order to**

configure a cacheable view of the source and destination memory units" (Column 4, lines 12) and explains that when a transfer of data from one memory location to another is requested, a CPU transfers or copies the data completely within the cache (Figure 3 and Column 7, lines 47-58)].

Fuhijira discloses "with the first controller monitoring operation of the processor to terminate the transmission of the data to the second randome access memory location, during transmission of the quantity thereto, in response to the processor generating a write request to the second random memory location" as **["during the DMA transfer between two memories, it is possible to make a normal interruption of the DMA transfer as if the interrupt request signal DONE is generated, by making a write operation with respect to the register 18 from the CPU 50" and explains "in this state where the DMA transfer is made.. the CPU 50 outputs the chip select signal CS responsive to an external interrupt request. In a step S1, the CPU 50 discriminates whether or not a write operation is made with respect to the register 18... when the discrimination result in the step S1 becomes YES, the data handler 17 in a step S2 supplies the terminate request signal CLS to the request handler 15" (Col. 6, lines 13-21; Col. 5, lines 49-64; Figure 5 and related text)]**.

Garret et al. (US 6,408,369), McKenney (US 6,230,241) and Fujihira et al. (US 5,278,965) are analogous art because they are from the same field of memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the internal memory transfer system which uses a controller to perform memory transfer/copy operations as taught by Garret, further perform these

operations in a random access volatile memory instead of performing the transfers within permanent storage as taught by McKenney, and further cancel DMA transmission of data when a write request has been generated as taught by Fujihira.

The motivation for doing so would have been because McKenney teaches that performing a transfer or copy of data completely within a cache instead of permanent storage provides **["a very high speed data transfer" (Column 7, lines 48-58) and also explains that by performing memory transfers within cache, a system can achieve "greater data transfer throughput between a source and one or more destinations" (Column 2, lines 56-58)]** and Fujihira also teaches **["according to the direct memory access controller of the present invention, it is possible to make a normal termination during a direct memory access transfer regardless of whether or not a memory involved in the direct memory access transfer has a function of generating a normal termination request signal. Further the normal termination request signal can be made at an arbitrary timing" (Col. 2, lines 6-28)]**.

Therefore, it would have been obvious to combine Fujihira et al. (US 5,278,965) with McKenney (US 6,230,241) and Garret et al. (US 6,408,369) for the benefit of performing internal memory transfers to obtain the invention as specified in claims 1 and 22.

5. As per **claim 2**, the combination of Garret, McKenney and Fujihira discloses "a computer system" **[See rejection to claim 1]** "wherein said random access memory is coupled to said data communications facility via a memory controller, said memory controller configured to manage operations for said random access memory" **[With respect to this limitation, Garret discloses Busses connecting "memory controller**

14" to "tapes 18a-18k" and busses connecting "memory controller 14" to "disk drives 16a-a6k" (Figure 1)].

6. As per **claims 3 and 24**, the combination of Garret, McKenney and Fujihira discloses "a computer system" **[See rejection to claims 1 and 22 above]** "wherein the data is copied from the first random access memory location to the second random access memory location by an internal memory transfer" **[Garret discloses this limitation as it is taught that "the transfer is made internally of the storage controller rather than requiring the command processors to communicate directly with each other" (Columns 1-2, lines 65-67 and 1)]**

"without traveling over the data communications facility" **[With respect to this limitation, Garret discloses that "the busses connecting the host computer to the disk drive controller are also not used and remain free for other operations" (Column 3, lines 48-50)].**

7. As per **claim 4**, the combination of Garret, McKenney and Fujihira discloses "a computer system" **[See rejection to claim 1]** "wherein said first controller is provided by said memory controller" **["Memory controller 14" (Figure 1)].**

8. As per **claim 9,** the combination of Garret, McKenney and Fujihira discloses "a computer system" **[See rejection to claim 1]** "wherein the first controller maintains a record of copy operations that are currently in progress" **[With respect to this limitation, Garret discloses that a controller sets "a state of the pending stored data as a write pending state" and later "destages the write pending memory stored data to the second storage device" (Column 1, lines 40-45) as a way for the controller of keeping a record and control of the operations currently being processed].**

9. As per **claims 10 and 25**, the combination of Garret, McKenney and Fujihira discloses "a computer system" **[See rejection to claims 1 and 22 above]** "wherein the processor ~~is allowed to continue~~ continues processing operations prior to ~~completion of the copy~~ data being completely copied to the second random access memory location" **[Garret discloses "a command processor host computer with the additional selected ability to transfer data without itself being involved in the physical transfer process" (Column 2, lines 6-9) because "controller 14" is in charge of the transfer of data (Column 1, lines 53-54)].**

10. As per **claims 14 –15 and 29**, the combination of Garret, McKenney and Fujihira discloses "a computer system" **[See rejection to claims 1 and 22 above]** "further comprising a cache" **[With respect to this limitation, Garret teaches that "The storage system, according to the invention, features a storage controller having a cache memory" (Column 1, lines 46-47)]**. McKenney discloses, "any cache entry for the second random access memory location is invalidated in response to said single command" by a processor as **["the CPU prepared the destination block in the cache to receive the data. This is done by instructing the cache to empty the contents of the destination block" and explains that the contents of a destination block are "flushed or cleared so that the next step does not need to be concerned with the contents" of a destination block before performing a transfer (Column 7, lines 36-47)]**.

11. As per **claims 16 and 30**, the combination of Garret, McKenney and Fujihira discloses the system/method of claims 14 and 29 **[See rejection to claims 14 and 22 above]** McKenney discloses a system and method for updating the data stored in cache memory "wherein any updated cache entry for the first random access memory location

is flushed to memory in response" to a memory transfer. as **["the CPU instructs the cache to empty the contents of source address block corresponding to the location of I/O memory that is to be read" and explains that "The source location in the cache is flushed before the read to ensure that whatever data is in the cache at this location is written out to its respective memory location before the data to be transferred is brought in" (Columns 6-7, lines 66-67 and 1-8)]**.

12. As per **claim 17**, the combination of Garret, McKenney and Fujihira discloses "a computer system" **[See rejection to claim 1 above]** "wherein said processor supports a specific programming command to copy data from a first random access memory location to a second random access memory location" **[With respect to this limitation, Garret discloses a method that "features receiving an internal copy command from a commanding processor over a controller" (Column 1, lines 38-39); this command comprising a "transfer of physical data from a first storage device to a second storage device" (Column 1, lines 33-35)]**.

13. As per **claim 18**, the combination of Garret, McKenney and Fujihira discloses "a computer system" **[See rejection to claim 1]** "wherein said data communications facility is a bus" **["Busses 36," "busses" connecting "memory controller 14" to "tapes 18a-18k" and "busses" connecting "memory controller 14" to "disk drives 16a-16k" (Figure 1)]**.

14. As per **claims 19 and 23**, the combination of Garret, McKenney and Fujihira discloses "a computer system" **[See rejection to claims 1 and 22 above]** "wherein said bus supports a command set, and said single command is part of said command set" **[With respect to this limitation, Garret discloses that "the host computer sends a**

system command over a channel, the SCSI channel or the fiber channel" (Column 3, lines 51-54)].

15. As per **claim 20**, the combination of Garret, McKenney and Fujihira discloses "a computer system" **[See rejection to claim 1]** "wherein said first controller transmits an acknowledgement of said single command back to the processor, and wherein the processor is responsive to a failure to receive said acknowledgement within a predetermined time-out period to perform said copy operation by issuing separate read and write commands" **[With respect to this limitation, Garret discloses that "the controller returns a *command not completed* back to the host computer and the host computer can either try the operation again, or transfer the data using a *prior art* command sequence" (Columns 3-4, lines 66-67 and 1-3) where the "*prior art* command sequence" involves "reading data from one disk drive unit into its own memory and then writing the data from its own memory to a second disk drive unit" (Column 1, lines 14-16)].**

16. **Claims 5-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Garret et al. (US 6,408,369), McKenney (US 6,230,241) and Fujihira et al. (US 5,278,965) as applied to claims **1-4, 9-10, 14-20 ,22-25 and 29-30** above, and further in view of Busser et al. (US 6,732,243).

17. As per **claims 5 and 8**, the combination of Garret, McKenney and Fujihira discloses "a computer system" as disclosed in claim 1 **[See rejection to claim 1 above]** but does not disclose expressly that "a first portion of random access memory is coupled to said data communications facility via a first memory controller and includes said first random access memory location, and a second portion of random access memory is

coupled to said data communications facility via a second memory controller and includes said second random access memory location."

Busser discloses a system and method where "a first portion of memory is coupled to said data communications facility via a first memory controller and includes said first memory location, and a second portion of memory is coupled to said data communications facility via a second memory controller and includes said second memory location". Busser teaches a **[method and apparatus for mirroring data in a storage system (Column 4, lines 44-45)]** including **["a first controller management module" (Column 4, lines 45-46) and "a second controller management module" (Column 4, lines 51-52) wherein the "first controller memory module" has "a first memory" (Column 13, lines 63-67) and the "second controller memory module" has "a second memory" (Column 14, lines 1-3)]**. Busser also teaches that **["data is mirrored from the first controller management module to the second controller management module" (Column 4, lines 48-61)]** and that **[the controllers are connected to a bus (Column 2, line 12)]**.

Garret et al. (US 6,408,369), McKenney (US 6,230,241), Fujihira et al. (US 5,278,965) and Busser et al. (US 6,732,243) are analogous art because they are from the same field of endeavor of copying/transferring data from one memory location to another.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to make the system for transferring data from one memory location to another as taught by Garret, transfer data within a random access volatile memory as taught by McKenney, cancel DMA transmission of data when a write request has been

generated as taught by Fujihira and further include two different controllers, one controlling a first memory location and the other controlling a second memory location, as described by Busser.

The motivation for doing so, as taught by Busser, would have been that by having two different "controller management modules" controlling each of two different memory locations, **["data is mirrored from the first controller management module to the second controller management module using the first direct memory access engine while avoiding interruption to the second processor" (Column 4, lines 58-61) and vice versa]**. Busser also teaches that this approach is useful because it **["reduces the processing overhead involved with mirroring data" (Column 4, lines 38-39)]**.

Therefore, it would have been obvious to combine Busser et al. (US 6,732,243) with Garret et al. (US 6,408,369), McKenney (US 6,230,241) and Fujihira et al. (US 5,278,965) for the benefit of creating a system and method for transferring data from one memory location to another to obtain the invention as specified in claims 5 and 8.

18. As per **claims 6 and 7**, the combination of Garret, McKenney, Fujihira and Busser discloses "a computer system/method" according to claim 5 **[See rejection to claim 5 above]** "wherein ~~the~~ data is copied from the first random access memory location to the second random access memory location by using a peer-to-peer copy operation on the data communication facility" and "wherein said data communications facility supports direct memory access (DMA), and said peer-to-peer copy operation is performed by using a transaction analogous to DMA." Busser teaches a system to transfer data from one memory location to another that uses **["DMA mirroring;" he also explains that "DMA is a capability provided by some computer bus architectures"**

(Column 10, lines 18-28)]. Busser further explains that having a "data mirroring system" that uses "DMA transfer" allows for faster processing because **[it does not consume the computer's processing resources (Column 10, lines 25-28)]**.

19. **Claims 11-12 and 26-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Garret et al. (US 6,408,369), McKenney (US 6,230,241) and Fujihira et al. (US 5,278,965) as applied to claims **1-4, 9-10, 14-20, 22-25 and 29-30** above, and further in view of O'Brien et al. (US 6,038,639).

20. As per **claims 11 and 26**, the combination of Garret, McKenney and Fujihira discloses a computer system according to claim 10 **[See rejection to claim 10 above]** but does not disclose expressly that "the first controller redirects a read request for the second random access memory location to the first random access memory location if the copy has not yet completed."

O'Brien discloses a system for transferring data from one memory location to another wherein "the controller redirects a read request for the second memory location to the first memory location if the copy has not yet completed." O'Brien teaches this limitation as it is explained that **["a request to read data from the copy data file received before the mapping table pointers have been updated is redirected to the original data file" (Column 4, lines 40-43)]**.

Garret et al. (US 6,408,369), McKenney (US 6,230,241), Fujihira et al. (5,278,965) and O'Brien et al. (US 6,038,639) are analogous art because they are form the same field of endeavor of copying/transferring data from one memory location to another.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to make the system for transferring data from one memory location to another as described by Garret, transfer data within a random access volatile memory as taught by McKenney, cancel DMA transmission of data when a write request has been generated as taught by Fujihira, further provide a method so that once a copy command is issued by a processor; any read command to the destination location is redirected to the source location as long as the copy operation has not been completed, as taught by O'Brien.

The motivation for doing so would have been because O'Brien teaches that any read command to the destination location is redirected to the source location as long as the copy operation has not been completed **["to ensure that the data file read operation behaves as though the snapshot copy process had been completed" (Column 4, lines 40-44) in order to guarantee "copy data file correspondence to the original data file" (Column 4, lines 49-50)]**.

Therefore, it would have been obvious to combine O'Brien et al. (US 6,038,639) with Garret et al. (US 6,408,369), McKenney (US 6,230,241) and Fujihira et al. (US 5,278,965) for the benefit of creating a system and method to copy/transfer data from one memory location to another as specified in claims 11 and 26.

21. As per **claims 12 and 27**, the combination of Garret, McKenney and Fujihira teaches a system as specified in claim 10 **[See rejection to claim 10 above]**. O'Brien discloses that "the controller delays a write request for the first random access memory location pending completion of the copy" as it is taught that **["Any attempt to update the mapping table to reflect data written to the original data file of the copy data file**

that occurs after initiation of the snapshot copy operation must wait until the first set of mapping table pointers have been updated" (Column 3, lines 26-30)].

VIII. RELEVANT ART CITED BY THE EXAMINER

22. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

23. The following reference teaches interrupting ordered copying in response to a write request.

US 2002/0073090

IX. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

24. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

25. Per the instant office action, claims 1-12, 14-20, 22-27 and 29-30 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

27. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 31, 2006

Yaima Campos
Examiner
Art Unit 2185

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
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